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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,701	02/19/2004	Iwao Sugiura	042113	3201
38834	7590	06/16/2006	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			WARREN, MATTHEW E	
		ART UNIT	PAPER NUMBER	
			2815	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/780,701	SUGIURA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 22 March 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,2,4,5,7 and 9-21 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2,4,5,7 and 9-21 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 22 March 2006 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

This Office Action is in response to the Amendment filed on March 22, 2006.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 2, 4, 5, and 7-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites the limitation "said electrode pad" in line 14. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 4, 5, 7-9, and 13-16, as far as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga (US 6,670,710 B2) in view of Nakajima et al. (US 2003/0230809 A1).

In re claim 1, Matsunaga shows (figs. 1-3) a semiconductor device comprising a substrate (11); a first multilayer interconnection structure (13, 14, 16, 18) formed on said

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substrate; and second multilayer interconnection structure (19, 22) formed on said first multilayer interconnection structure, said first multilayer interconnection structure including a first interlayer insulation film (13, 14, 16, 18) and a first interconnection layer (not labeled and next to layers 15, 17) included in said first interlayer insulation film; said second multilayer interconnection structure including a second interlayer insulation film (19, 22) and a second interconnection layer (not labeled and next to layers 20, 21) included in said second interlayer insulation film, said first multilayer interconnection structure including a pillar (30) extending from a surface of said substrate and reaching at least said second multilayer interconnection structure, said first interconnection layer being formed so as to avoid said pillar. Matsunaga shows that there is an electrode pad area (35/36) formed above the substrate but does not specifically show the pillar being formed in a region of the substrate right underneath the electrode pad. Nakajima et al. shows (fig. 1) a semiconductor device in which dummy plugs/pillars are formed underneath an electrode pad (36). With such a configuration, the pillars (16D, 24D, 26D, and 34D) provide mechanical support and reinforcement to the electrode pad (36) during a wire bonding process. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electrode pad of Matsunaga by forming pillars under the electrode pad as taught by Nakajima to provide mechanical support and reinforcement to the electrode pad.

In re claim 2, Matsunaga shows (figs. 1-3) that said pillar has a layered structure identical to a layered structure of said first interconnection layer in said first multilayer interconnection structure.

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In re claim 4, Matsunaga shows (figs. 1-3) that said pillar has an edge part engaging to a bottom surface (17) of said second multilayer interconnection structure.

In re claim 5, Matsunaga shows (figs. 1-3) that said pillar extends further in said second multilayer interconnection structure and has a layered structure identical to a layered structure of said second interconnection layer in a part thereof extending in said second multilayer interconnection structure.

In re claim 7, Matsunaga shows (figs. 1-3) an electrode pad (46) is formed on said second multilayer interconnection structure.

In re claim 8, the references do not specifically disclose that the plural numbers of pillars occupy at least 15% of the area. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the pillars in a desired amount suitable for the electrode pad reinforcement, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

In re claim 9, Matsunaga shows (figs. 1-3) that there is formed an active device (12) in region of said substrate right underneath said electrode pad.

In re claim 13, Matsunaga does not specifically disclose said pillar has a Young modulus of 30GPa or more. However, the pillar inherently has such a property since it has the same structure and materials as the instant invention.

In re claim 14, Matsunaga shows (figs. 1-3) that in said first multilayer interconnection structure, said pillar is formed with plural numbers so as to be located at

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both sides of an interconnection pattern forming a part of said first interconnection layer

Figure 1, shows an overhead view in which the pillar (30) surrounds the devices region.

In re claims 15 and 16, Matsunaga shows (fig. 1) that said pillar (30) forms a wall extending continuously on said surface of said substrate. The pillar extends continuously along a circumference of said substrate in said first and second multilayer interconnection structures and form a guard ring.

Claims 10-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga (US 6,670,710 B2) in view of Nakajima et al. (US 2003/0230809 A1) as applied to claim 1 above, and further in view of the Applicant's Prior Art Figures 1-4 (APAF).

In re claims 10-12 and 17-19 concerning the first and second interlayer insulating films each having a desired Young's Modulus, Matsunaga and Nakajima do not disclose those properties of the film. However, the APAF 1 shows that a first interlayer insulating film (14-17) and a second interlayer insulating film (18-21) each have the desired properties of the claimed invention in that the first film has Young's Modulus lower than the Young's Modulus of the second film. The specification on pages 7-12 lists all of the properties of the first interlayer insulating film of the porous organic film and the second interlayer insulating film of a CVD material. With such a configuration, the semiconductor device combined with the metallization structure has reduced signal delay and high speed operation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulation

materials of Matsunaga and Nakajima by using the low Young's Modulus first interlayer insulation film and the higher Young's Modulus second interlayer insulation film as taught by the APAF to form a device having reduced signal delay and high speed operation.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga (US 6,670,710 B2) in view of Nakajima et al. (US 2003/0230809 A1) as applied to claim 1 above, and further in view of Pio (US 6,815,328).

In re claim 20, Matsunaga and Nakajima show all of the elements of the claims except said pillar being provided on a device isolation structure on said substrate. Pio shows (fig. 8) that an interconnect pillar structure (31b, 38, 56, etc.) is formed on a device isolation region (26). With this configuration, the interconnection structure utilizes all of the available space on the substrate, thus the interconnect wiring density can be increased without increasing the size of the substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pillar structure of Matsunaga and Nakajima by forming the pillars on the device isolation region as taught by Pio to form an interconnection structure utilizing all of the available space on the substrate and increasing the interconnect wiring density.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga (US 6,670,710 B2) in view of Nakajima et al. (US 2003/0230809 A1) as

applied to claim 1 above, and further in view of Sugiyama et al. (US Pub. 2002/0040986 A1).

In re claim 20, Matsunaga and Nakajima show all of the elements of the claims except said pillar is provided in plural number on said substrate, and wherein there is formed a reinforcement structure in said first multilayer interconnection structure so as to extend diagonally between said plural pillars. Sugiyama et al. shows (fig. 7) a more detailed interconnection layout in which the interconnect structure (104) is formed diagonally in the multilayered structure of layers 88, 90, and 92 and within the boundaries of the pillar structure (102 and 106). While Sugiyama only discloses this configuration to form a specific connection scheme in the interconnect structure, it is inherent that such a structure also provides reinforcement to the interlayer insulation. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the interconnect of Matsunaga and Nakajima by forming the interconnects in a diagonal configuration as taught by Sugiyama to form a specific routing scheme.

#### ***Response to Arguments***

Applicant's arguments filed with respect to claims 1, 2, 4, 5 and 7-21 have been fully considered but they are not persuasive. The applicant primarily asserts that Matsumura and Nakajima et al. cannot be combined because the via ring of Matsumura is not analogous to the wire bonding process cited in Nakajima. The examiner believes that the references can be combined and that the combination shows all of the elements

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of the claims. As stated in the rejection above, Matsumura already shows that there is an electrode pad area formed over the substrate but the pad is formed inside of the region of the via ring/pillars. Therefore, Matsumura was deficient in showing that the via ring/pillars are formed under an electrode pad. Nakajima was cited to cure the deficiencies of Matsumura by showing that dummy vias or plugs could be formed underneath an electrode pad to provide mechanical support. Therefore, Matsumura would be modified to form the electrode pad above or directly over the via rings/pillars to provide mechanical support to the electrode pad. Matsumura is particular relevant to this concept since Matsumura already discloses that the "via ring 81 is intended to prevent cracks at the time of scribing" (col. 2, lines 32-35). Thus, forming the electrode pad directly over the vias/pillars would also prevent cracks during a wire bonding process (as taught by Nakajima). Therefore, the prior art references are combinable and show all of the elements of the claims. This action is made final.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

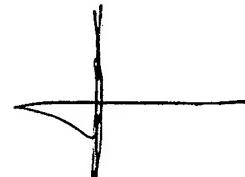
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MEW  
*MEW*  
June 8, 2006



KENNETH PARKER  
SUPERVISORY PATENT EXAMINER